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SAXENA, AKASH

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/943,595	SWOBODA, GARY L.
	Examiner	**Art Unit**	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *10 July 2006*.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-4,16,17 and 27-54* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-4,16,17 and 27-54* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

   1. ☐ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____.

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 16-17, and 27-54 have been presented for examination based on the

   application filed on 10th July 2006.

2. Claim(s) 1 is/are amended.

3. The arguments submitted by the applicant have been fully considered. Claims 1-4,

   16-17, and 27-54 remain rejected. The examiner's response is as follows.

4. This action is made FINAL.

Response to Applicant's Remarks & Examiner's Withdrawals

5. Examiner respectfully withdraws the claim rejection(s) under 35 USC § 112 to

   claim(s) 1-4, 16-17, and 27-54 in view of the applicant's arguments.

6. Examiner maintains the claim rejection(s) under 35 USC § 101 to claim(s) 1-4, 30-31

   and 37-42 in view of the amendment and/or applicant's arguments.

Response to Applicant's Remarks for 35 U.S.C. § 102/103

7. **Claim 1-4, 16-17, 27-29, 34, 37-39, 43-45, and 49-51 were rejected under <u>35</u>**

<u>U.S.C. 103(a)</u> as being unpatentable over US Patent No 6,732,307 issued to

Edwards.

<u>Regarding Claim 1, 16 and 27</u>

Applicant has argued that Edwards fails to disclose the recited relationship between

the data sizes and the respective clock rates.

The limitation is being discussed is as follows:

> "outputting the sequence of second information blocks via a plurality of terminals at a
> transmission clock rate, <u>said first fixed size</u>, <u>said data processor clock rate</u>, <u>said second fixed size</u>
> and <u>said transmission clock rate</u> <u>related whereby</u> <u>a bit rate of first information blocks</u> <u>equals</u> <u>the</u>
> <u>bit rate of said second information blocks</u>."

Examiner has presented a 102/103 rejection here (as one reference 103). Examiner

has shown that Edwards teaching make the above limitation obvious (Edwards:

Col.2 Lines 37-40, 23-26 and 40-58). Starting with Edwards Col.2 Lines 37-40:

> In another aspect, the trace information includes timing information. In one aspect, the trace
> system *may be* <u>used as a rate converter for converting a transmission rate of messages</u>
> <u>transmitted to a memory system on-chip or an external system</u>.

This above teaches a rate conversion system, i.e. where the input bit rate <u>may differ</u>

from the output bit rate. The input bit rate <u>equaling</u> output bit rate would be the trivial

solution and would be obvious to one or ordinary skill. Also, if desired the

functionality of rate converter is indicated to be optional (use of may be) and may be

removed to give equaling input (processor) and output (transmission) bit rate. MPEP

2144.04 II states: Omission of an Element and Its Function Is Obvious If the unction

of the Element Is Not Desired. See In re Larson,340 F.2d 965, 144 USPQ 347

(CCPA 1965) In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975).

Further, Edwards references an interface to an external system where the rate

conversion is happening prior to transmission. Applicant has stated there is no

reference "transmission circuit 215". Applicant did not cite this section (Col.2 Line

37-40).

Edwards Col.2 Lines 23-26 states:

> Specifically, <u>the trace system includes devices,</u> which <u>operate separately from the processor,</u> operate at internal clock speeds of the processor, or operate in modes wherein the loss of trace information does not affect processor operation.

As taught above, Edwards clearly distinguishes between the data processor clock

rate and the transmission clock rate (part of the trace circuit).

Edwards Col.2 Lines 40-58 states:

> In another aspect, the <u>trace information may be compressed by the trace system.</u> By compressing information, ***trace information is preserved for transmission over lower-bandwidth*** <u>links and maximizes on-chip trace storage.</u> For example, trace information may be compressed by <u>compressing timestamp and address information.</u> Further, trace information may be compressed by <u>omitting duplicate types of information,</u> such as one trace packet of a particular operation type. Also, <u>information may be filtered</u> by predefining criteria upon which trace information is generated. By filtering information and eliminating duplicate information on-chip, bandwidth requirements of links to external systems and on-chip storage requirements are reduced. A trace message may be <u>compressed by replacing an absolute value</u> of a data field in the message with a relative value. Periodic reference messages including absolute values of compressed information may be provided to provide a reference for the relative value.

As taught above, Edwards address the limitation relating to the first fixed size

(information form the data processor) and the second fixed size (processed

information to be transmitted). Edwards even goes further to detail various ways of

compression thereby first fixed size (information form the data processor) and the

second fixed size (processed information to be transmitted) would differ in size to

meet the bit rate requirement of a <u>lower bandwidth medium</u>. To tie the above three

cited sections for example - <u>said first fixed size (10bit),</u> <u>said data processor clock</u>

<u>rate (10 Hz),</u> <u>said second fixed size</u> (6 bit) and <u>said transmission clock rate</u> (6 Hz)

related whereby a bit rate of first information blocks (10 bit/10 Hz = 1 bit/Hz) equals

the bit rate of said second information blocks (6 bit/6 Hz = 1 bit/Hz)." - due to

compression from 10 bit to 6 bit of the fixed size blocks. Hence all the references to

other instances of the transmission circuit are not required as the teaching of the

limitation is already present in section cited by the examiner and made obvious.

Applicant's argument for claims 1, 16 and 27 are found to be unpersuasive.

Regarding Claim 2, 17 and 34

Claim 2 depends from claim 1. It is shown above that Edwards (Col.2 Lines 40-58)

teaches first fixed size is compressed to form of second fixed size. It is generally well

understood and obvious in the art compression, that the compressed data is differs

in size from the uncompressed data and is smaller in size. Further, the sections cited

in Edwards are to show the difference in size between the transmitted data & data

received from the processor and not the mechanism of the process. Examiner

respectfully maintains the rejection in view of the clarification above.

Regarding Claim 37, 43 and 49

Examiner agrees with the applicant that Edwards does not teach the transmission

clock rate greater than the data processor clock rate. However the rejection is now

made under 35 USC 103/102, and Edwards discloses a broader teaching of rate

converter, where the rate is a programmable factor as described by Microsoft

dictionary (Definition for Communication controller/parameters). It would be obvious

to one skilled in the art to choose from various rate conversion factors (greater or

lesser) based on the design choice, as the basic teaching or rate converter is

already present in Edwards. Microsoft dictionary defines the communications

controller & communications parameters as follows:

> Communications controller: A device used as an intermediately in transferring communications to and from the host computer to which it is connected. [...]. A communications controller can be either programmable machine in its own right or a non-programmable device designed to follow a certain communications protocols.
>
> Communications Parameters: Any of the several settings required in order to enable computers to communicate. In asynchronous communications, for example, modem speed _(transmission rate)_, number of data bits and stop bits, and type of parity are parameters that must be set correctly to establish communications between two modems.

Section cited (Edwards: Col.2 Lines 23-26) clearly indicates that the transmission

clock rate is operated independently from processor clock rate. This does not inhibit

the transmission clock to be dependent (lesser/equal/greater in rate) on processor

clock. As indicated above clock rate is programmable. Rejection is respectfully

maintained.

Regarding Claim 39, 45, 51

Although the trace processor 205 may not be running at or from the processor clock

frequency 218, or the multiples there of, the pre-scalar section is used to

determining the interval when the trace is captured and stamps it accordingly based

on the time difference. The trace in effect even if transmitted (outputted) at a

different (transmission rate) rate is captured & time-stamped based on the pre-scalar

clock (a value less than processor clock rate).

Further, even if for argument sake, the reference is read differently, the limitation

regarding "transmission rate less than processor clock rate", would be obvious for

the same reasons as cited for claim 37, 43 and 49 above. Arguments regarding

claim 1, 16 and 27 are already addressed above. Arguments presented against this

combination are found to be unpersuasive and respective rejections are maintained.

Response to Applicant's Remarks for 35 U.S.C. § 103

8. **Claims 30, 32 and 35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards in view of Teich.**

Regarding Claim 30, 32 and 35

Examiner agrees with the applicant that the rejection as presented does not make sense. Further, examiner acknowledges that the reference was misinterpreted thereby resulting in typographical error.

The **Teich** reference should have read as said first size (Teich: Fig.9 Local data package) is an integral multiple of the said second data size (Teich: Fig.9 ATM Cell). The said first size is Local data package because they are still in the system (processor/trace system before transmission) and the said second data size is ATM Cell because these cells are being transmitted (like the said second data size blocks). Since the clarification of same reference reads on the presented claim limitations, the rejection is maintained.

9. **Claims 31, 33 & 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards, in view of Baldwin.**

Regarding Claim 31, 33 and 36

Examiner agrees that LLC packets are not first fixed size packets, however the limitation directed more towards non-integral disassembly of the first size packets into second fixed size packets (ATM packets) which is clearly taught by Baldwin. Edwards reference is relied upon meet the limitation of first fixed size packets. Further, it would be obvious to one of ordinary skill in the art that any system that

has capability to handle variable first fixed size packets (like LLC packets) will be able to handle fixed size packets, thereby meeting functionality required by the limitations. Further, In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Further, applicant argues that clearly teaches ATM Cells include bits not within the original LLC packets and this clearly contrary to the above quote limitations of claim 31, 33 and 36.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., second fixed size packets cannot have bits other than the ones present in the first fixed size packets) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Arguments presented against this combination are found to be unpersuasive and rejection is maintained.

10. Claim 40-42, 46-48 & 52-54 were rejected under 35 U.S.C. 103(a) as being

unpatentable over Edwards, in view of Baldwin, further in view Horie.

<u>Regarding Claim 40-42, 46-48 & 52-54</u>

Applicant has argued that neither Edwards-Baldwin nor Horie disclose conditions

under which the selection of the bits for the second information blocks stalls.

Examiner respectfully disagrees, Edwards and Horie both teach stalling under various

circumstances. E.g. stalling of operation in case of inability to transmit (due to buffer

overflow) (Edwards: Fig.2 Elements 219 and 202); sending reference bits after stall

(Edwards: Table 7/8); NOP bits as pseudo-transmission data transmission, indicating

that no data is being transmitted and for synchronization purpose (Horie: Fig.3C; Col.6

Lines 25-34). Applicant's argument regarding establishing a prima facie case of

obviousness are considered and are found to be unpersuasive.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claim 1-4, 30-31, 37-42 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Regarding Claim 1

Method claim 1 does not recite a tangible result to the preamble disclosing "exporting emulation information from the data processor" as the last step outputs the second sequence of second information blocks, but that information is not tangibly stored in any location once derived from the first information block. Hence, there is no indication there the results of outputting step are tangible.

Examiner suggests that the following modification (underlined) can overcome the deficiency cited above:

"outputting a sequence of second information blocks from the data processor integrated circuit and stored on a host via a plurality of terminals....".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claim 1-4, 16-17, 27,-29, 34, 37-39, 43-45, and 49-51 are rejected under 35

U.S.C. 103(a) as being unpatentable over US Patent No 6,732,307 issued to

Edwards.

Regarding Claim 1

Edwards teaches a method of exporting emulation information from a data processor

integrated circuit (Edwards: Col. 2, Lines 31-33; *Col.1 Line 13-14 – SOC, 56-57-*

ICE), comprising collecting internal emulation information from a data processor at a

data processor clock rate (Edwards: Col. 2, Lines 12-19); arranging the collected

emulation information into a plurality of first information blocks having a first fixed

size (Edwards: Col. 17, Lines 45-52).

Edwards teaches receiving the plurality of first information blocks (Edwards: Col. 17,

Lines 45-52 in trace buffer 227) and arranging (e.g. PC compression) the emulation

information contained therein into a plurality of second information blocks (Edwards:

having a second fixed size which differs from the first fixed size of the first

information blocks as data received from the trace buffer 227 (representing the first

information block) is formatted to include time stamp information and stored in FIFO

(Edwards: Col. 7, Lines 27-31; Fig.2, Element 202) and compression being ·

performed on the PC (Edwards: Fig 11A & 11B) which *obviously* changes the size of

the information block. FIFO is storage sequential storage element re-presenting

second information block, which differ in size from trace data information.

Edwards teaches outputting a sequence of the second information blocks *from the*

data processor integrated circuit *(Fig.2 element 102)* via a plurality of terminals at a

transmission clock rate, which may be different from the processor clock rate as obvious from the rate converter teaching of Edwards (Edwards: Col.2 Lines 37-40, 40-58), said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks.

Applicant has presented arguments (Remarks: Pg. 19) that block size of the information in the trace buffer 227 is the same as FIFO 202 & trace port registers 212. Examiner respectfully disagrees, as Edwards explicitly teaches change in first fixed size as present in the trace buffer 227 by addition of information size (timestamp & address by the trace processor 205 & reference counter 217; Col.19 Lines 64-67; Col.20 Lines 1-7) and further teaches compression of the PC and other information (Edwards: Fig 11A &11B; Col.19 Lines 3-19). Further, Table 7(sic) 8 (Col.20) clearly shows the reference message sent out having 14 bytes content, which is different in size from the message size present the trace buffer 227 (8 bytes to max 24 bytes).

Edwards does not explicitly teach said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of one skilled in the art of "data rate transmission and manipulation" and Edwards to relate the processor rate and first fixed size to transmission rate and second fixed size as basic input output

equation of any rate converter system taught by Edwards (Edwards: Col.2 Lines 37-
40; _23-26_) which as Edwards teaches is necessary to maximize the use of the
limited transmission bandwidth to external systems (Edwards: Col.2 Lines 40-58)
with additional information added to first fixed size (e.g. timestamp, address).

Regarding Claim 2

Edwards teaches second fixed size (Edwards: Col.20 Table 8 7(sic)) is smaller in
size than the first fixed size (Edwards: Trace Buffer 227 Max 3*8bytes; Col. 17,
Lines 45-52).

Regarding Claim 3

Edwards teaches that trace information present in the FIFO might contain other
control information like timing, program counter and address data in a compressed
format (Edwards: Col.18, Lines 44-49). An embodiment of compression code is also
shown (Edwards: Col.19, Lines 20-59). This data is exported the debug tool on the
external system (Edwards: Col.6, Lines 33-35) the tool reconstructs the message
and control information (Edwards: Col.19, Lines 18-20).

Regarding Claim 4

Edwards teaches that first information block may be packets on a switched
communication medium (Edwards: Col.5, Lines 43-46) and second information
blocks are made from first information blocks and are inform of packets (Edwards:
Col.8, Lines 58-60; Col.7, Lines 31-38) to be sent to an external system over a
transmission circuit.

Regarding Claim 16

Apparatus of claim 16 performs and is directed at the same functionality as the

method of claim 1 and is thus rejected in the like manner. A data processor in the

claim 16 is equivalent to data processor in claim 1. A collector in claim 16 is

performing the same step of the method as the collection process in the claim 1. An

exporter in claim 16 (coupled to the collector) performs the function of receiving

trace data (from collector) and re-arranging trace data, as in method-step of claim 1.

An exporter coupled to plurality of terminals to output the data is performing the

same function as "outputting in sequence" step in claim 1. Further claim 16 states

that all these components are part of an integrated circuit. Edwards teaches that

data processor, collector and exporter can be on the same integrated circuit

(Edwards: Fig.1, Element 101). The added limitations are also addressed similarly

as in claim 1.

Regarding Claim 17

Claim 17 discloses similar limitations as claim 2 and is rejected for the same reasons

as claim 2.

Regarding Claim 27

System of claim 27 performs and is directed at the same functionality as the method

of claim 1 and is thus rejected in the like manner. Edwards teaches that data

processor (Edwards: Fig.1, Element 102), emulation controller (Edwards: Fig.1,

Element 103-Debug unit), apparatus to convey emulation information between

processor and emulation controller (Edwards: Fig.2, Element 227 (trace buffer),

220(capture buffer), 206(trace data latch)) and exporter (Edwards: Fig.2, Element

215, 106) can be on the same integrated circuit (Edwards: Fig.1, Element 101).

An exporter coupled to plurality of terminals to exporter the data is performing the

same function as "outputting information" step in claim 1. The added limitations are

also addressed similarly as in claim 1.

Regarding Claims 28 & 29

Teachings of Edwards are disclosed above in claims 27. Edwards also teaches that

the debug system (emulation controller) is connected to external system (Edwards:

Col.6, Lines 12-14). An external system could be a host computer running the debug

tool mentioned by Edwards (Edwards: Col 7, Lines 46-48). A keyboard constitutes a

"tactile interface" and a computer monitor constitutes a "visual interface". Official

notice is taken that it is extremely well known in the art to use a keyboard and a

computer monitor with a computer (host interface) to form a man-machine interface.

Regarding Claim 34

Claim 34 discloses similar limitations as claim 2 and is rejected for the same reasons

as claim 2.

Regarding Claim 37

Edwards also teaches rate conversion system (Edwards: Col.2 Lines 36-40) making

the transmission speed variable and adjustable. Further, Edwards teaches that trace

system (transmission clock) operate independent to the internal clock speed of the

processor (Edwards: Col.2 Lines 23-27), whereby the transmission speed is design

choice. Microsoft dictionary defines the communications controller &

communications parameters as follows:

> Communications controller: A device used as an intermediately in transferring communications to and from the host computer to which it is connected. [...]. A communications controller can be either programmable machine in its own right or a non-programmable device designed to follow a certain communications protocols.

> Communications Parameters: Any of the several settings required in order to enable computers to communicate. In asynchronous communications, for example, modem speed *(transmission rate)*, number of data bits and stop bits, and type of parity are parameters that must be set correctly to establish communications between two modems.

It would be obvious to one skilled in the art of communications that the transmission

rate conversion is a design choice known to the designer.

Regarding Claim 38

As indicated the by Edwards the fixed size of the trace may be at the maximum of

3*64 bit in the trace buffer 227, i.e. trace buffer may occupy only one slot (8 bytes)

(Edwards: Fig.8 Elements 808-810). Further, Edwards teaches trace messages

(second fixed size) in byte increments, which are greater in size than 8 bytes

(Edwards: Tables 4-8) thereby teaching second fixed size greater than first fixed

size.

Regarding Claim 39

Edwards teaches transmission clock rate is less than data processor clock rate

(Edwards: Col.8 Lines 30-45) where the clock frequency is divided and fed to the

trace processor, thereby reducing the effective transmission frequency. Further,

Edwards also teaches rate conversion system (Edwards: Col.2 Lines 36-40) making

the transmission speed variable and adjustable.

Regarding Claims 43-45

Claims 43-45 disclose similar limitations as claims 37-39 respectively and are

rejected for the same reasons as claim 37-39 respectively.

Regarding Claims 49-51

Claims 49-51 disclose similar limitations as claims 37-39 respectively and are

rejected for the same reasons as claim 37-39 respectively.

13. **Claims 30,32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. US Patent No 6,732,307 issued to Edwards in view of U.S. Patent No. 6229808 issued to Teich et al (Teich hereafter).**

Regarding Claims 30

Teaching of Edwards relating to collection of trace information in first fixed size and second fixed size is provided in respective parent and/or independent claim rejection in previous office action. Edwards teaches current packet register as target port registers (Fig.2 Element 212).

Edwards does not teach the new limitations where the second fixed size information block "is" and "is not" in multiples of first information blocks explicitly. Further, Edwards also does not explicitly teach arranging and selecting the bits from the first fixed size and vise versa.

Teich teaches a first fixed size (Teich: Fig.9 ATM Cells) is an integral multiple of second fixed size (Teich: Fig.9 Local Data Package). The selecting and arranging is obvious in the design as for conversion between ATM package and Local package (Teich: Fig.9; Col.5 Lines 50-Col.6Lines21) would necessitate the need for selecting bits.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Teich to Edwards to convert the first fixed block of information into second fixed block of information. The motivation to combine would have been that Teich simplifies the design of packet

switching by providing little or no translation of data while changing from one fixed

size to another (Teich: Col.1 Lines 46-50).

Regarding Claim 32

Claim 32 disclose similar limitations as claims 30 respectively and are rejected for

the same reasons as claim 30.

Regarding Claim 35

Claim 35 disclose similar limitations as claims 30 respectively and are rejected for

the same reasons as claim 30.

14. Claims 31, 33 & 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. US Patent No 6,732,307 issued to Edwards, in view of U.S. Patent No. 5,953,339 issued to Baldwin al (Baldwin hereafter).

Regarding Claims 31

Teaching of Edwards relating to collection of trace information in first fixed size and second fixed size is provided in respective parent and/or independent claim rejection in previous office action. Edwards teaches current packet register as target port registers (Fig.2 Element 212).

Edwards does not teach the new limitations where the second fixed size information block "is" and "is not" in multiples of first information blocks explicitly. Further, Edwards also does not explicitly teach arranging and selecting the bits from the first fixed size and vise versa including the use of last and current packet register.

Baldwin teaches a first fixed size (Teich: Fig.1 LLC packets) is a forming a *non-integral multiple of second fixed size* (Teich: Fig.1 ATM packets). The selecting and arranging is obvious in the design as for conversion between ATM packets and LLC packets (Teich: Fig.9; Col.5 Lines 50-Col.6Lines21) would necessitate the need for selecting bits and remembering last LLC packet bits.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Baldwin to Edwards. The motivation to combine would have been that Baldwin teaches better compaction technique instead of bit stuffing technique used in alternate implementation when the

inter-packet conversion sizes are non-integral multiples. The advantages of compaction and bit stuffing technique are well known in the art.

Regarding Claim 33

Claim 33 disclose similar limitations as claims 31 respectively and are rejected for the same reasons as claim 31.

Regarding Claim 36

Claim 36 disclose similar limitations as claims 31 respectively and are rejected for the same reasons as claim 31.

15. Claim 40-42, 46-48 & 52-54 are rejected under 35 U.S.C. 103(a) as being

unpatentable over US Patent No 6,732,307 issued to Edwards, in view of U.S.

Patent No. 5,953,339 issued to Baldwin al (Baldwin hereafter), further in view

of U.S. Patent No. 5,790,398 issued to Horie (Horie hereafter).

Regarding Claim 40-42

Teachings of Edwards & Baldwin are shown in the claim 31 rejection above.

Edwards teaches stalling of operation in case of inability to transmit (due to buffer

overflow) (Edwards: Fig.2 Elements 219 and 202).

Edwards and Baldwin do not teach use of NOP bit if no first information block is

available for transmission.

Horie teaches use of NOP bits as pseudo-transmission data transmission,

indicating that no data is being transmitted and for synchronization purpose (Horie:

Fig.3C; Col.6 Lines 25-34). It would be obvious to use the NOP when no data is

present to be transmitted from the teachings of Horie and initializing the NOP bits in

first information block.

Motivation to combine Edwards with Baldwin is presented above claim 31

rejection above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at

the time the invention was made to apply the teachings of Horie to Edwards &

Baldwin. The motivation to combine would have been that Edwards teaches

synchronization when the references are not absolute values (Edwards: Col.20

Lines 7-33) and Horie teaches synchronization through the NOP operation to stop

the performance from deteriorating (Horie: Col.2 Lines 3-14; Col.6 Lines 25-34).

Regarding Claims 46-48

Claims 46-48 disclose similar limitations as claims 40-42 respectively and are

rejected for the same reasons as claim 40-42 respectively.

Regarding Claims 52-54

Claims 52-54 disclose similar limitations as claims 40-42 respectively and are

rejected for the same reasons as claim 40-42 respectively.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and

any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing

date of the advisory action. In no event, however, will the statutory period for reply

expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Akash Saxena whose telephone number is (571) 272-

8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).

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Thursday, September 14, 2006

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